

Home | Login | Logout | Access Information | Ale

	Xplore®		Welcome United St	ates Patent and Trac	lemark Office		
☐ Search Results		_	BROWS	SE SEA	ARCH	IEEE XPLORE GUIDE	
Your search ma	insulated <sentence>transistor tched 22 of 231 documents. I00 results are displayed, 25 to a</sentence>						<b>⊡</b> e-mail
» Search Optior	ns	Modify S	Search				
View Session H	istory	((((insula	ted <sentence>transisto</sentence>	r? and evaluat* <paragra< td=""><td>ph&gt;transistor?)<and< td=""><td>&gt;(insula Search &gt;</td><td></td></and<></td></paragra<>	ph>transistor?) <and< td=""><td>&gt;(insula Search &gt;</td><td></td></and<>	>(insula Search >	
New Search		C ch	eck to search only with	nin this results set			
» Key		Display	Format:	Citation C Cit	ation & Abstract		
,	IEEE Journal or Magazine IEE Journal or Magazine	<b>√</b> view	selected items	Select All Desel	ect All		
	IEEE Conference Proceeding	<b></b>	1. Three-Dimension	al Simulation of VLS	SI MOSFET's: The	Three-Dimensional Sim	ulation Progra
	IEE Conference Proceeding	<b>J</b> !	Husain, A.; Cham	berlain, S.G.;			_
	IEEE Standard			s, IEEE Journal of 2, Apr 1982 Page(s)	:261 - 268		
			AbstractPlus   Full Rights and Permis	Text: <u>PDF(</u> 1480 KB) ssions	IEEE JNL	•	
			Tsai, HH.; Chen, <u>Electron Devices</u> , Volume 35, Issue Digital Object Ider	SM.; Chen, HB.; V IEEE Transactions or 3, March 1988 Page htflier 10.1109/16.245 I Text: PDF(1008 KB)	Vu, CY.; 1 e(s):275 - 284 1	/nMOSFET fabrication	
			Heremans, P.; Be <u>Electron Devices</u> , Volume 35, Issue Digital Object Ider	ol for the hot-carrier illens, R.; Groeseneke IEEE Transactions or 12, Dec 1988 Page ntifier 10.1109/16.879 I Text: <u>PDF</u> (1580 KB)	n, G.; Maes, H.E.; 1 s):2194 - 2209 4	channel and p-channel M	MOSFETS
•			Rights and Permis	ssions		·	
			Electron Devices, Volume 35, Issue	SFET lifetime under K.; Lee, P.M.; Choi, J. IEEE Transactions or 7, Part 1, July 1988 htifier 10.1109/16.335	Y.; Ko, P.K.; Hu, C 1 · Page(s):1004 - 10	.;	
			AbstractPlus   Ful Rights and Permi	Text: <u>PDF</u> (596 KB) ssions	IEEE JNL		
		D	MOSFETs Shiuh-Wuu Lee; Electron Devices, Volume 41, Issue	ased method for exp LEEE Transactions of 3. March 1994 Page ntifier 10.1109/16.275	<u>1</u> e(s):403 - 412	ination of metallurgical	channel length

	AbstractPlus   Full Text: PDF(760 KB) IEEE JNL Rights and Permissions
	<ol> <li>MOSFET effective dimensions determination for VLSI process evaluation         Tuinhout, H.P.;         <u>Microelectronic Test Structures, 1989, ICMTS 1989, Proceedings of the 1989 International Confere</u>         13-14 March 1989 Page(s):61 - 64         Digital Object Identifier 10.1109/ICMTS.1989.39282     </li> </ol>
	AbstractPlus   Full Text: PDF(216 KB) IEEE CNF Rights and Permissions
	7. Measurement of Minimum-Geometry MOS Transistor Capacitances Paulos, J.J.; Antoniadis, D.A.; Solid-State Circuits. IEEE Journal of Volume 20. Issue 1, Feb 1985 Page(s):277 - 283
	AbstractPlus   Full Text: PDF(1128 KB) IEEE JNL Rights and Permissions
<u>Г</u>	8. Radiation-Induced changes in floating-body phenomena in SOI MOSFET's Ouisse, T.; Ghibaudo, G.; Brini, J.; Cristoloveanu, S.; Borel, G.; Nuclear Science, IEEE Transactions on Volume 39, Issue 3, Part 1-2, June 1992 Page(s):372 - 375 Digital Object Identifier 10.1109/23.277520
	AbstractPlus   Full Text: PDF(248 KB) IEEE JNL Rights and Permissions
	9. Hot carrier evaluation of MOSFETs in ULSI circuits using the photon emission method Uraoka, Y.; Tsutsu, N.; Morii, T.; Tsuji, K.;  Electron Devices, IEEE Transactions on Volume 40, Issue 8, Aug. 1993 Page(s):1426 - 1431  Digital Object Identifier 10.1109/16.223701
	AbstractPlus   Full Text: PDF(624 KB)   IEEE JNL Rights and Permissions
	10. Application specific 1200V planar and trench IGBTs  Shenoy, P.M.; Shekhawat, S.; Brockway, B.;  Applied Power Electronics Conference and Exposition, 2006, APEC '06, Twenty-First Annual IEEE 19-23 March 2006 Page(s):5 pp.  Digital Object Identifier 10.1109/APEC.2006.1620532  AbstractPlus   Full Text: PDE(332 KB)   IEEE CNF
	Rights and Permissions
	11. A systematic hard- and soft-switching performances evaluation of 1200 V punchthrough IGE Azzopardi, S.; Vinassa, JM.; Woirgard, E.; Zardini, C.; Briat, O.;  Power Electronics, IEEE Transactions on  Volume 19, Issue 1, Jan. 2004 Page(s):231 - 241  Digital Object Identifier 10.1109/TPEL.2003.820580
	AbstractPlus   References   Full Text: <u>PDF</u> (976 KB)   IEEE JNL Rights and Permissions
П	12. Carrier mobility and current saturation in the MOS transistor Hofstein, S.R.; Warfield, G.; Electron Devices, IEEE Transactions on Volume 12, Issue 3, Mar 1965 Page(s):129 - 138
	AbstractPlus   Full Text: PDF(1064 KB)   IEEE JNL   Rights and Permissions
<u> </u>	13.

	Sah, C.T.; Pao, H.C.; <u>Electron Devices, IEEE Transactions on</u> Volume 13, Issue 4, Apr 1966 Page(s):393 - 409
	AbstractPlus   Full Text: PDF(1936 KB) IEEE JNL Rights and Permissions
	14. Subthreshold current of dual-gate MOSFET's  Barsan, R.M.;  Electron Devices, IEEE Transactions on  Volume 29, Issue 10, Oct 1982 Page(s):1516 - 1522  AbstractPlus   Full Text: PDE(736 KB)   IEEE JNL  Rights and Permissions
	15. Design and Characteristics of the Lightly Doped Drain-Source (LDD) Insulated Gate Field-Efi Ogura, S.; Tsang, P.J.; Walker, W.W.; Critchlow, D.L.; Shepard, J.F.; Solid-State Circuits, IEEE Journal of Volume 15, Issue 4, Aug 1980 Page(s):424 - 432  AbstractPlus   Full Text: PDE(1600 KB)   IEEE JNL Rights and Permissions
	16. Numerical and experimental comparison of vertical DMOSFET and UMOSFET Chang, HR.: Temple, V.A.K.; Baliga, B.J.;  Electron Devices, IEEE Transactions on Volume 35, Issue 12, Dec 1988 Page(s):2459 - 2460  Digital Object Identifier 10.1109/16.8904  AbstractPlus   Full Text: PDF(180 KB) IEEE JNL Rights and Permissions
	17. A closed-loop evaluation and validation of a method for determining the scattering limited c.  MOSFETs  Lee, SW.; Chan, TY.;  Electron Devices, IEEE Transactions on  Volume 37, Issue 11, Nov. 1990 Page(s):2388 - 2394  Digital Object Identifier 10.1109/16.62297  AbstractPlus   Full Text: PDF(588 KB)   IEEE JNL-  Rights and Permissions
in the second se	18. Observation of MOSFET degradation due to electrical stressing through gate-to-source and capacitance measurement Yeow, Y.T.; Ling, C.H.; Ah, L.K.; Electron Device Letters. IEEE Volume 12, Issue 7, July 1991 Page(s):366 - 368 Digital Object Identifier 10.1109/55.103609  AbstractPlus   Full Text: PDF(200 KB) IEEE JNL Rights and Permissions
	19. Performance of thin-film transistors on polysilicon films grown by low-pressure chemical va various pressures  Dimitriadis, C.A.; Coxon, P.A.; Dozsa, L.; Papadimitriou, L.; Economou, N.;  Electron Devices. IEEE Transactions on  Volume 39, Issue 3, March 1992 Page(s):598 - 606  Digital Object Identifier 10.1109/16.123484  AbstractPlus   Full Text: PDE(780 KB) IEEE JNL  Rights and Permissions
Ū	20. New generation 1200 V power module with trench gate IGBT and super soft recovery diode a Lwamoto, H.; Kawakami, A.; Satoh, K.; Takahashi, H.; Nakaoka, M.; Electric Power Applications, IEE Proceedings-

	Digital Object Identifier 10.1049/ip-epa:20000331
	AbstractPlus   Full Text: PDF(600 KB)   IEE JNL
j j	21. Temperature dependence of drain-induced barrier lowering in deep submicrometre MOSFET Fikry, W.; Ghibaudo, G.; Dutoit, M.;  Electronics Letters  Volume 30, Issue 11, 26 May 1994 Page(s):911 - 912  AbstractPlus   Full Text: PDF(164 KB) IEE JNL
	22. Conduction in ohmic region of submicrometre MOSFET Tong, K.Y.; Circuits. Devices and Systems, IEE Proceedings G Volume 136, Issue 5, Oct 1989 Page(s):260 - 262
	AbstractPlus   Full Text: PDF(156 KB)   IEE JNL

indexed by indexed by inspec\*

Copyright 2006 IE



Home | Login | Logout | Access Information | Ale

#### Welcome United States Patent and Trademark Office

] Search Results	BROWSE SEARCH IEEE XPLORE GUIDE
Your search matched 16 of 22 documents.	a page, sorted by Relevance in Descending order.
» Search Options	
View Session History	Modify Search  ((((((insulated <sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insulated<sentence>transistor? and evaluat*</sentence></and></paragraph></sentence>
New Search	((((((insulated <sentence>transistor? and evaluat*<paragraph>transistor?)<and>(insul</and></paragraph></sentence>
	Check to search only within this results set
» Кеу	Display Format:
IEEE JNL IEEE Journal or Magazine	view selected items   Select All Deselect All
IEE JNL IEE Journal or Magazine	view selected items  Select All Deselect All
IEEE CNF IEEE Conference Proceeding	1. An evaluation of FUROX isolation technology for VLSI/nMOSFET fabrication
IEE CNF IEE Conference Proceeding	Tsai, HH.; Chen, SM.; Chen, HB.; Wu, CY.;
IEEE STD IEEE Standard	Electron Devices, IEEE Transactions on  Volume 35, Issue 3, March 1988 Page(s):275 - 284  Digital Object Identifier 10.1109/16.2451
	AbstractPlus   Full Text: PDF (1008 KB) IEEE JNL Rights and Permissions
	2. Three-Dimensional Simulation of VLSI MOSFET's: The Three-Dimensional Simulation Progra Husain, A.; Chamberlain, S.G.;  Solid-State Circuits, IEEE Journal of Volume 17, Issue 2, Apr 1982 Page(s):261 - 268  AbstractPlus   Full Text: PDF(1480 KB) IEEE JNL Rights and Permissions
	3. Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs Heremans, P.; Bellens, R.; Groeseneken, G.; Maes, H.E.;  Electron Devices, IEEE Transactions on Volume 35, Issue 12, Dec 1988 Page(s):2194 - 2209 Digital Object Identifier 10.1109/16.8794
	AbstractPlus   Full Text: <u>PDF</u> (1580 KB) IEEE JNL Rights and Permissions
	4. A capacitance-based method for experimental determination of metallurgical channel length MOSFETs Shiuh-Wuu Lee: Electron Devices. IEEE Transactions on Volume 41, Issue 3, March 1994 Page(s):403 - 412 Digital Object Identifier 10.1109/16.275227
	AbstractPlus   Full Text: PDF(760 KB) IEEE JNL Rights and Permissions
	5. Measurement of Minimum-Geometry MOS Transistor Capacitances Paulos, J.J.; Antoniadis, D.A.; Solid-State Circuits. IEEE Journal of Volume 20, Issue 1, Feb 1985 Page(s):277 - 283
	AbstractPlus   Full Text: PDF(1128 KB)   IEEE JNL

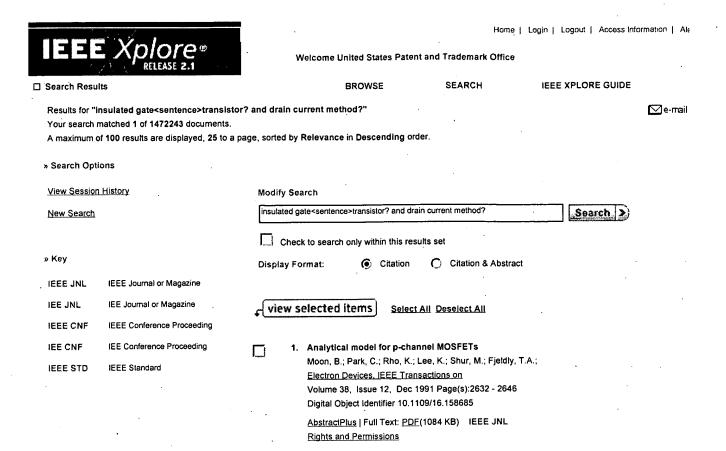
### Rights and Permissions

	6.	Radiation-induced changes in floating-body phenomena in SOI MOSFET's Ouisse, T.; Ghibaudo, G.; Brini, J.; Cristoloveanu, S.; Borel, G.; Nuclear Science, IEEE Transactions on Volume 39, Issue 3, Part 1-2, June 1992 Page(s):372 - 375
		Digital Object Identifier 10.1109/23.277520 <u>AbstractPlus</u>   Full Text: <u>PDF</u> (248 KB) IEEE JNL <u>Rights and Permissions</u>
	<b>7.</b>	A systematic hard- and soft-switching performances evaluation of 1200 V punchthrough IGE Azzopardi, S.; Vinassa, JM.; Woirgard, E.; Zardini, C.; Briat, O.; Power Electronics. IEEE Transactions on Volume 19, Issue 1, Jan. 2004 Page(s):231 - 241 Digital Object Identifier 10.1109/TPEL.2003.820580
		AbstractPlus   References   Full Text: PDF (976 KB)   IEEE JNL   Rights and Permissions
	8.	Carrier mobility and current saturation in the MOS transistor Hofstein, S.R.; Warfield, G.; Electron Devices. IEEE Transactions on Volume 12, Issue 3, Mar 1965 Page(s):129 - 138
	•	AbstractPlus   Full Text: PDF(1064 KB)   IEEE JNL   Rights and Permissions
anna c	<b>9.</b>	The effects of fixed bulk charge on the characteristics of metal-oxide-semiconductor transis Sah, C.T.; Pao, H.C.; <u>Electron Devices, IEEE Transactions on</u> Volume 13, Issue 4, Apr 1966 Page(s):393 - 409 <u>AbstractPlus   Full Text: PDF(1936 KB)   IEEE JNL Rights and Permissions</u>
Ė		0. Subthreshold current of dual-gate MOSFET's  Barsan, R.M.; <u>Electron Devices, IEEE Transactions on</u> Volume 29, Issue 10, Oct 1982 Page(s):1516 - 1522
		AbstractPlus   Full Text: PDF (736 KB) IEEE JNL Rights and Permissions
	1	<ol> <li>Design and Characteristics of the Lightly Doped Drain-Source (LDD) Insulated Gate Field-Eft Ogura, S., Tsang, P.J., Walker, W.W., Critchlow, D.L., Shepard, J.F., Solid-State Circuits, IEEE Journal of Volume 15, Issue 4, Aug 1980 Page(s):424 - 432</li> </ol>
		AbstractPlus   Full Text: PDF(1600 KB) IEEE JNL Rights and Permissions
<u>.</u>	1	2. Numerical and experimental comparison of vertical DMOSFET and UMOSFET Chang, HR.; Temple, V.A.K.; Baliga, B.J.;  Electron Devices. IEEE Transactions on Volume 35, Issue 12, Dec 1988 Page(s):2459 - 2460  Digital Object Identifier 10.1109/16.8904
		AbstractPlus   Full Text: PDF(180 KB) IEEE JNL Rights and Permissions
		Performance of thin-film transistors on polysilicon films grown by low-pressure chemical va various pressures Dimitriadis, C.A.; Coxon, P.A.; Dozsa, L.; Papadimitriou, L.; Economou, N.;
		Electron Devices IEEE Transactions on

	Digital Object Identifier 10.1109/16.123484
	AbstractPlus   Full Text: PDF(780 KB) IEEE JNL Rights and Permissions
	14. Temperature dependence of drain-induced barrier lowering in deep submicrometre MOSFET Fikry, W.; Ghibaudo, G.; Dutoit, M.; <u>Electronics Letters</u> Volume 30, Issue 11, 26 May 1994 Page(s):911 - 912
٠.	AbstractPlus   Full Text: PDF(164 KB)   IEE JNL
	15. Conduction in ohmic region of submicrometre MOSFET Tong, K.Y.; Circuits, Devices and Systems, IEE Proceedings G Volume 136, Issue 5, Oct 1989 Page(s):260 - 262
	AbstractPlus   Full Text: PDF(156 KB) IEE JNL
	16. Application specific 1200V planar and trench IGBTs Shenoy, P.M.; Shekhawat, S.; Brockway, B.; Applied Power Electronics Conference and Exposition, 2006, APEC '06. Twenty-First Annual IEEE 19-23 March 2006 Page(s):5 pp. Digital Object Identifier 10.1109/APEC.2006.1620532
	AbstractPlus   Full Text: PDF(332 KB) IEEE CNF Rights and Permissions

Volume 39, Issue 3, March 1992 Page(s):598 - 606

indexed by 词 Inspec\*



indexed by
inspec\*

Help Contact Us Privac

© Copyright 2006 IE



Subscribe (Full Service) Register (Limited Service, Free) Login

Search: • The ACM Digital Library • The Guide

insulated gate type transistor?<sentence>evaluat\* and channel





Feedback Report a problem Satisfaction survey

Terms used

insulated gate type transistor? sentence evaluat and channel width and drain current method?

Found 43,842 of 196,780

Sort results

by

Display results

relevance

expanded form

Save results to a Binder ? Search Tips

Open results in a new

Try this search in The ACM Guide

Try an Advanced Search

window

Results 1 - 20 of 200

Result page: 1 2 3 4 5 6 7 8 9 10

next

Relevance scale

Best 200 shown

A static power model for architects

J. Adam Butts, Gurindar S. Sohi

December 2000 Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture MICRO 33

**Publisher: ACM Press** 

Full text available: pdf(136.88 KB)

ps(431.76 KB)

Additional Information: full citation, references, citings, index terms

**Publisher Site** 

Double-gate SOI devices for low-power and high-performance applications

K. Roy, H. Mahmoodi, S. Mukhopadhyay, H. Ananthan, A. Bansal, T. Cakici

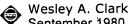
May 2005 Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05

Publisher: IEEE Computer Society

Full text available: 📆 pdf(783.31 KB) Additional Information: full citation, abstract

Double-gate (DG) transistors have emerged as promising devices for nano-scale circuits due to their better scalability compared to bulk CMOS. Among the various types of DG devices, quasi-planar SOI FinFETs are easier to manufacture compared to planar doublegate devices. DG devices with independent gates (separate contacts to back and front gates) have recently been developed. DG devices with symmetric and asymmetric gates have also been demonstrated. Such device options have direct implications ...

From Electron Mobility to Logical Structure: A View of Integrated Circuits



September 1980 ACM Computing Surveys (CSUR), Volume 12 Issue 3

Publisher: ACM Press

Full text available: pdf(3.29 MB)

Additional Information: full citation, references, citings, index terms

Power reduction techniques for microprocessor systems Vasanth Venkatachalam, Michael Franz September 2005 ACM Computing Surveys (CSUR), Volume 37 Issue 3





**Publisher: ACM Press** 

Full text available: pdf(602.33 KB) Additional Information: full citation, abstract, references, index terms

Power consumption is a major factor that limits the performance of computers. We survey the "state of the art" in techniques that reduce the total power consumed by a microprocessor system over time. These techniques are applied at various levels ranging from circuits to architectures, architectures to system software, and system software to applications. They also include holistic approaches that will become more important over the next decade. We conclude that power management is a ...

**Keywords**: Energy dissipation, power reduction

5 Managing leakage power: Analysis and minimization techniques for total leakage



considering gate oxide leakage

Dongwoo Lee, Wesley Kwong, David Blaauw, Dennis Sylvester June 2003 Proceedings of the 40th conference on Design automation DAC '03

Publisher: ACM Press

Full text available: pdf(217.28 KB)

Additional Information: full citation, abstract, references, citings, index terms

In this paper we address the growing issue of gate oxide leakage current (Igate) at the circuit level. Specifically, we develop a fast approach to analyze the total leakage power of a large circuit block, considering both Igate and subthreshold leakage (Isub). The interaction between Isub and Igate complicates analysis in arbitrary CMOS topologies and we propose simple and accurate heuristics based on table look-ups to quickly estimate the state-dependent total leakage current within 1% of SPICE ...

6 Delay optimization of combinational static CMOS logic





M. Hofmann, J. K. Kim

October 1987 Proceedings of the 24th ACM/IEEE conference on Design automation **DAC '87** 

Publisher: ACM Press

Full text available: pdf(864.63 KB)

Additional Information: full citation, abstract, references, citings, index

Several methods for increasing the speed of combinational static CMOS circuits, including techniques for partitioning gates on the basis of circuit complexity and input arrival time, are described. The target layout style is standard cell, rather than a PLA or gate matrix scheme. Use of a standard-cell-like image allows a two-level buffered hierarchy to be introduced which is beneficial to reducing circuit delays. Preliminary results from device sizing algorithms are also given. The device ...

Is nanoelectronics the future of microelectronics?



Mark Lundstrom

August 2002 Proceedings of the 2002 international symposium on Low power electronics and design ISLPED '02

Publisher: ACM Press.

Full text available: pdf(241.10 KB) Additional Information: full citation, abstract, references, index terms

We examine current research in nanoelectronics and discuss the role it may play in future electronic systems.

Keywords: Moore's Law, molecular electronics, nanoelectronics

Deep Sub-Micron IDDQ Testing: Issues and Solutions

M. Sachdev

March 1997 Proceedings of the 1997 European conference on Design and Test EDTC

**Publisher: IEEE Computer Society** 

Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, citings Publisher Site

The effectiveness of I/sub DDQ/ testing in deep sub-micron is threatened by the increased transistor sub-threshold leakage current. In this article, we survey possible solutions and propose a deep sub-micron I/sub DDQ/ test mode. The methodology provides means for unambiguous measurements of I/sub DDQ/ components and defect diagnosis. The effectiveness of the test mode is demonstrated with a real life example.

Keywords: CMOS integrated circuits, deep submicron IDDQ testing, transistor subthreshold leakage current, defect diagnosis, CMOS IC

Layout tools for analog ICs and mixed-signal SoCs: a survey

Rob A. Rutenbar, John M. Cohn

May 2000 Proceedings of the 2000 international symposium on Physical design ISPD '00

Publisher: ACM Press

Full text available: pdf(247.03 KB) Additional Information: full citation, references

10 Emerging technologies and designs for low power: Analysis of super cut-off

transistors for ultralow power digital logic circuits

Arijit Raychowdhury, Xuanyao Fong, Qikai Chen, Kaushik Roy

October 2006 Proceedings of the 2006 international symposium on Low power electronics and design ISLPED '06

Publisher: ACM Press

Full text available: 📆 pdf(340.59 KB) Additional Information: full citation, abstract, references, index terms

Super cut-off devices with sub-60mV/decade subthreshold swings have recently been demonstrated and being extensively studied. This paper presents a feasibility analysis of such tunneling devices for ultralow power subthreshold logic. Analysis shows that this device can deliver 800X higher performance (@iso-IOFF) compared to a MOSFET. The possible use of this device as a sleep transistor in conjunction with the regular Si MOSFET shows 2000X average improvement in leakage power compared to Si MOSF ...

Keywords: carbon nanotube FETs, tunneling transistors

11 Spin MOSFETs as a basis for spintronics

Satoshi Sugahara, Masaaki Tanaka

May 2006 ACM Transactions on Storage (TOS), Volume 2 Issue 2

Publisher: ACM Press

Full text available: 🔁 pdf(427.11 KB) Additional Information: full citation, abstract, references, index terms

This article reviews a recently proposed new class of spin transistors referred to as spin metal-oxide-semiconductor field-effect transistors (spin MOSFETs), and their integrated circuit applications. The fundamental device structures, operating principle, and theoretically predicted device performance are presented. Spin MOSFETs potentially exhibit significant magnetotransport effects, such as large magneto-current, and also satisfy important requirements for integrated circuit applications suc ...



**Keywords**: MOSFETs, Spintronics, spin MOSFETs, spin transistors

12 Technologies and devices for low power: Modeling and analysis of total leakage



currents in nanoscale double gate devices and circuits

Saibal Mukhopadhyay, Keunwoo Kim, Ching-Te Chuang, Kaushik Roy

August 2005 Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05

**Publisher: ACM Press** 

Full text available: pdf(485.85 KB) Additional Information: full citation, abstract, references, index terms

In this paper we model (numerically and analytically) and analyze sub-threshold, gate-tochannel tunneling, and edge direct tunneling leakage in Double Gate (DG) devices. We compare the leakage of different DG structures, namely, doped body symmetric device with polysilicon gates, intrinsic body symmetric device with metal gates and intrinsic body asymmetric device with different front and back gate material. It is observed that, use of (near-mid-gap) metal gate and intrinsic body devices signif ...

Keywords: SRAM, double-gate devices, estimation, gate leakage, quantum effect, stacking effect, subthreshold leakage

13 Low power circuits and microarchitectures: Utilizing reverse short channel effect for



optimal subthreshold circuit design

Tae-Hyoung Kim, Hanyong Eom, John Keane, Chris Kim

October 2006 Proceedings of the 2006 international symposium on Low power electronics and design ISLPED '06

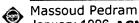
Publisher: ACM Press

Additional Information: full citation, abstract, references, index terms Full text available: pdf(1.93 MB)

The impact of the Reverse Short Channel Effect (RSCE) on device current is stronger in the subthreshold region due to the reduced Drain-Induced-Barrier-Lowering (DIBL) and the exponential dependency of current on threshold voltage. This paper describes a device size optimization method for subthreshold circuits utilizing RSCE to achieve high drive current, low device capacitance, less sensitivity to random dopant fluctuations, and better subthreshold swing. Simulation results using ISCAS benchma ...

Keywords: PVT variations, digital circuits, optimization, reverse short channel effect, subthreshold circuits, subthreshold operation

14 Power minimization in IC design: principles and applications



January 1996 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 1 Issue 1

Publisher: ACM Press

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(550.02 KB)

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

**Keywords:** CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

15 A set of programs for MOS design

G. Sakauye, A. Lubiw, J. Royle, R. Epplett, J. Twidale, E. Shew, E. Attfield, F. Brglez, P. Wilcox

June 1981 Proceedings of the 18th conference on Design automation DAC '81

Publisher: IEEE Press

Full text available: pdf(778.19 KB)

Additional Information: full citation, abstract, references, citings, index terms

A set of programs used in the design of custom hand packed and standard cell MOS circuits is described. The programs cover logic simulation, filter analysis, circuit simulation, timing simulation, circuit extraction from layout, design tolerance checking, connectivity checking and user interface facilities. A cell documentation system is used to tie together the various design support packages.

16 Power optimization of large-scale circuits: Analysis and optimization of gate leakage



current of power gating circuits

Hyung-Ock Kim, Youngsoo Shin

January 2006 Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06

Publisher: ACM Press

Full text available: pdf(151.22 KB) Additional Information: full citation, abstract, references

Power gating is widely accepted as an efficient way to suppress subthreshold leakage current. Yet, it suffers from gate leakage current, which grows very fast with scaling down of gate oxide. We try to understand the sources of leakage current in power gating circuits and show that input MOSFETs play a crucial role in determining total gate leakage current. It is also shown that the choice of a current switch in terms of polarity, threshold voltage, and size has a significant impact on total lea ...

17 Challenges and design choices in nanoscale CMOS



Siva G. Narendra

March 2005 ACM Journal on Emerging Technologies in Computing Systems (JETC),
Volume 1 Issue 1

Publisher: ACM Press

Full text available: pdf(5.35 MB) Additional Information: full citation, abstract, references, index terms

The driving force for the semiconductor industry growth has been the elegant scaling nature of CMOS technology. In this article, we will first review the history of technology scaling that follows Moore's law from the prespective of microprocessor designs. Challenges to continue the historical scaling trends will be highlighted and design choices to address two specific challenges, process variation and leakage power, will be discussed. In nanoscale CMOS technology generations, supply and thresh ...

Keywords: CMOS, leakage power, nanoscale, process variation

18 <u>Low power digital circuits design: Total leakage power optimization with improved mixed gates</u>



Frank Sill, Frank Grassert, Dirk Timmermann



September 2005 Proceedings of the 18th annual symposium on Integrated circuits and system design SBCCI '05

Publisher: ACM Press

Full text available: pdf(288.69 KB) Additional Information: full citation, abstract, references, index terms

Gate oxide tunneling current Igate and sub-threshold current Isub dominate the leakage of designs. The latter depends on threshold voltage Vth while Igate vary with the thickness of gate oxide layer Tox. In this paper, we propose a new method that combines approaches of Dual Threshold CMOS (DTCMOS), mixed-Tox CMOS, and pin-reordering. As the reduction of leakage leads to an increase of gate delay, our purpose is the reduction of total leakage at constant design performance. We modified a given t ...

**Keywords**: MVT, leakage currents, threshold voltage

19 Topological Analysis for Leakage Prediction of Digital Circuits

Wenjie Jiang, Vivek Tiwari, Erik de la Iglesia, Amit Sinha

January 2002 Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design ASP-DAC '02

Publisher: IEEE Computer Society

Full text available: pdf(115.48 KB)

Additional Information: full citation, abstract, citings

Publisher Site

Subthreshold leakage current is becoming an increasingly significant portion of the power dissipation in microprocessors due to technology and voltage scaling. Techniques to estimate leakage at the full chip level are indispensable for power budget allocation. In addition, simple and practical approaches and rules of thumb are needed to allow leakage to become part of the vocabulary of all designers. This paper focuses on the impact of circuit topology on leakage, which is often abstracted throu ...

20 Session 32: logic synthesis I: Gate sizing: finFETs vs 32nm bulk MOSFETs



Brian Swahn, Soha Hassoun

July 2006 Proceedings of the 43rd annual conference on Design automation DAC '06 Publisher: ACM Press

Full text available: pdf(800.60 KB) Additional Information: full citation, abstract, references, index terms

FinFET devices promise to replace traditional MOSFETs because of superior ability in controlling leakage and minimizing short channel effects while delivering a strong drive current. We investigate in this paper gate sizing of finFET devices, and we provide a comparison with 32nm bulk CMOS. Wider finFET devices are built utilizing multiple parallel fins between the source and drain. Independent gating of the finFET's double gates allows significant reduction in leakage current. We perform temper ...

**Keywords**: FinFET, gate sizing, thermal modeling

Result page: 1 2 3 4 5 6 7 8 9 10 Results 1 - 20 of 200

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2007 ACM, Inc. Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player



Login: 
Register

		, , , ,
Home	Browse Search Abstract Databases My Settings Alerts Help	
Quick Sear	n Title, abstract, keywords Author	
? search t	S Journal/book title Volume Issue F	Page
Add to r	Quick Links ,	
	s were found search tips link on the search form below for additional information.	
All Source	Journals Books Reference Works Abstract Databases Scirus	
	Enter terms using Boolean connectors (ex: cat OR feline AND nutrition)	Bas.
Term(s):	insulated gate type transistors	A d
	<b>Please Note</b> : ScienceDirect will migrate to a new search engine with a new search language as of 2 January 2007. All Search and Topic Alerts, Saved Searches and Saved Search Histories will be converted automatically to the new search language Read more As a result of the migration, Elsevier has decided to discontinue all the Abstract Databases on ScienceDirect Read more	21 and Ce d
Sources	☑ Journals ☑ Book Series ☑ Handbooks ☑ Reference Works ☐ Abstract Database	es
	select one or more:	
Subject:	- All Sciences - Agricultural and Biological Sciences	
	Arts and Humanities	
•	Biochemistry, Genetics and Molecular Biology  Hold down the Ctrl key (or # key) to select multiple entries.	
Dates:	<b>⊚</b> 1990 <b>©</b> to: 1999 <b>©</b> C All Years	Management of the second of th

## Search History - Turn On

Search >

Search for articles from our full-text collection and abstracts database using this search form. Click the **Help** button for step-by-step instructions on conducting a search using this form. Consult the Search Tips for information about the use of connectors, wildcards, and other search options which can improve the precision of your search.

Search Tips

Home Browse Search Abstract Databases My Settings Alerts Help

Clear

Recall Search



About ScienceDirect | Contact Us | Terms & Conditions | Privacy Policy

# Refine Search

### Search Results -

Term	Documents
YAMAGUCHI	39181
YAMAGUCHIS	. 0
INSULATED	215612
INSULATEDS	0
GATE	515963
GATES	238867
ТҮРЕ	3319059
TYPES	1668490
EVALUATION	348737
EVALUATIONS	43904
TRANSISTOR?	0
(YAMAGUCHI.IN. AND (INSULATED GATE TYPE TRANSISTOR? WITH EVALUATION) ).PGPB,USPT.	9

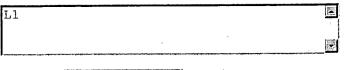
There are more results than shown above. Click here to view the entire set.

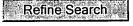
# US Pre-Grant Publication Full-Text Database US Patents Full-Text Database

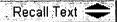
Database:

US OCR Full-Text Database EPO Abstracts Database JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins

~		1	
	MA		











## Search History

DATE: Friday, January 19, 2007

**Purge Queries** 

Printable Copy

Create Case

Set Name Query

Hit Count Set Name result set

side by side

DB=PGPB, USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ



Home | Login | Logout | Access Information | Ale

#### Welcome United States Patent and Trademark Office

☐ Search Session History

BROWSE

SEARCH

**IEEE XPLORE GUIDE** 

Fri, 19 Jan 2007, 11:40:03 AM EST

Edit an existing query or compose a new query in the Search Query Display.

#### Select a search number (#) to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Search Query Display

Berge Brown

#### **Recent Search Queries**

- #1 ((insulated gate type transistor?)<in>metadata)
- #2 insulated<sentence>transistor? and evaluat\*<paragraph>transistor?
- ((insulated<sentence>transistor? and evaluat\*<paragraph>transistor?)<AND>
  #3 (insulated gate<sentence>transistor? and evaluat\*<paragraph>transistor?
  <in>metadata))
- ((((insulated<sentence>transistor? and evaluat\*<paragraph>transistor?)<and>
  (insulated gate<sentence>transistor? and evaluat\*<paragraph>transistor?

  #4 <in>metadata())<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<and>on<an
- (((((((insulated<sentence>transistor?) and evaluat\*<paragraph>transistor?)<and>
  (insulated gate<sentence>transistor? and evaluat\*<paragraph>transistor?
  <in>metadata)))<and>((insulated<sentence>transistor? and
  evaluat\*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and
  evaluat\*<paragraph>transistor?<in>metadata))
  #5

  ((((insulated<sentence>transistor? and evaluat\*<paragraph>transistor?)<and>
  (insulated gate<sentence>transistor? and evaluat\*<paragraph>transistor?
  <in>metadata))<and>((insulated<sentence>transistor? and evaluat\*<paragraph>transistor? and
  evaluat\*<paragraph>transistor? and
  evaluat\*<paragraph>transistor? and
  evaluat\*<paragraph>transistor?<and>on evaluat\*<and color of the sentence>transistor? and
  evaluat\*</a><paragraph>transistor?<and color of the sentence>transistor? and
  evaluat\*</paragraph>transistor?<and color of the sentence>transistor?
- (insulated gate<sentence>transistor? and evaluat\*<paragraph>transistor?
  <in>metadata)))<and>((insulated<sentence>transistor? and
  evaluat\*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and
  evaluat\*<paragraph>transistor?>(in>metadata))
  #6

  (((insulated<sentence>transistor? and evaluat\*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and evaluat\*<paragraph>transistor?
  <in>metadata)))<and>((insulated<sentence>transistor? and evaluat\*<paragraph>transistor? and
  evaluat\*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and
  evaluat\*<paragraph>transistor?
  voltage)

((((((insulated<sentence>transistor? and evaluat\*<paragraph>transistor?)<and>

- ((((insulated<sentence>transistor? and evaluat\*<paragraph>transistor?)<and>
  (insulated gate<sentence>transistor? and evaluat\*<paragraph>transistor?

  #17 <in>metadata)))<and>(insulated<sentence>transistor? and
  evaluat\*<paragraph>transistor?)<and>(insulated gate<sentence>transistor? and
  evaluat\*<paragraph>transistor?<in>metadata)) and channel width)</a>
- #8 insulated gate<sentence>transistor? and drain current method?
- #9 insulated gate<sentence>transistor? and drain current method?

Hetp Contact Us Privac

& Copyright 2006 IE

<u>L1</u> yamaguchi.in. and (insulated gate type transistor? with evaluation) 9

<u>L1</u>

END OF SEARCH HISTORY

## **Hit List**

First Hit Clear Generate Collection Print Fwd Refs Bkwd Refs Generate OACS

Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 20040098681 A1

L1: Entry 1 of 9

File: PGPB

May 20, 2004

PGPUB-DOCUMENT-NUMBER: 20040098681

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040098681 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: May 20, 2004

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Yamaguchi, Kenji

Tokyo

JP

US-CL-CURRENT: 716/4

Full Title Citation Front	Review Classification Da	ate Reference	Sequences	Attachments	Claims	KAAC	Draw, De
						•	
							•

☐ 2. Document ID: US 20030113946 A1

L1: Entry 2 of 9

File: PGPB

Jun 19, 2003

PGPUB-DOCUMENT-NUMBER: 20030113946

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030113946 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: June 19, 2003

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Yamaguchi, Kenji

Tokyo

JΡ

US-CL-CURRENT: <u>438/17</u>

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KMC Draw De

☐ 3. Document ID: US 20020130679 A1

L1: Entry 3 of 9

File: PGPB

Sep 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020130679

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020130679 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION: .

NAME

CITY

STATE

COUNTRY

Yamaguchi, Kenji

Tokyo

JP

US-CL-CURRENT: 324/769

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KMC Draw. De

4. Document ID: US 20020127749 A1

L1: Entry 4 of 9

File: PGPB

Sep 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020127749

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020127749 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: September 12, 2002

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Yamaguchi, Kenji

Tokyo

JΡ

US-CL-CURRENT: 438/18; 438/17, 438/275

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims

5. Document ID: US 6727724 B2

L1: Entry 5 of 9

File: USPT

Apr 27, 2004

US-PAT-NO: 6727724

DOCUMENT-IDENTIFIER: US 6727724 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: April 27, 2004

INVENTOR-INFORMATION:

. NAME

CITY

STATE

ZIP CODE

COUNTRY

Yamaguchi; Kenji

Tokyo

JΡ

US-CL-CURRENT: 324/769; 324/719

Full Title Citation Front Review Classification Date Reference Common Action Claims KMC Draw De

☐ 6. Document ID: US 6649430 B2

L1: Entry 6 of 9

File: USPT

Nov 18, 2003

US-PAT-NO: 6649430

DOCUMENT-IDENTIFIER: US 6649430 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Yamaguchi; Kenji.

Tokyo

JΡ

US-CL-CURRENT: 438/17; 438/275

Full Title Citation Front Review Classification Date Reference Series Co. Attended Claims KMC Draw De

☐ 7. Document ID: US 6559672 B2

L1: Entry 7 of 9

File: USPT

May 6, 2003

US-PAT-NO: 6559672

DOCUMENT-IDENTIFIER: US 6559672 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: May 6, 2003

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Yamaguchi; Kenji

Tokyo

JΡ

US-CL-CURRENT: 324/769; 324/719

Full Title Citation Front Review Classification Date Reference Company Company Claims KMC Draw De

8. Document ID: US 6373274 B1

L1: Entry 8 of 9

File: USPT

Apr 16, 2002

US-PAT-NO: 6373274

DOCUMENT-IDENTIFIER: US 6373274 B1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: April 16, 2002

INVENTOR-INFORMATION:

NAME

CITY

STATE ZIP CODE

COUNTRY

Yamaguchi; Kenji

Tokyo

JΡ

US-CL-CURRENT: 324/769; 324/719

Full	Title	Citation	Front	Review	Classification	Date	Reference	19 8 10 6 11 18 25	Asielis	Claims	KWAC	Draw, De
		i					•					
·	т	`	4 ID.	110 61	60415 B1							

9. Document ID: US 6169415 B1

L1: Entry 9 of 9

File: USPT

Jan 2, 2001

US-PAT-NO: 6169415

DOCUMENT-IDENTIFIER: US 6169415 B1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: January 2, 2001

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Yamaguchi; Kenji

Tokyo

JP

US-CL-CURRENT: 324/769; 324/719

Full Title	Citation Front Review Classification Date Reference Sectionics (Attachin	ମନ୍ତି Claims KW	MC Draw. (
Clear	Generate Collection Print Fwd Refs Bkwd Refs	Generate	OACS
	<u> </u>	Documents	
	AMAGUCHI	39181	
	AMAGUCHIS	0	
·   —	ISULATED	215612	
1I	NSULATEDS	0	i
G <i>I</i>	ATE	515963	
G <i>I</i>	ATES	238867	
T	YPE	3319059	
T	YPES	1668490	

# **WEST Search History**

Hide Items Restore Clear Cancel

DATE: Friday, January 19, 2007

Hide?	Set Name	Query	Hit Count
	DB=PGPB	USPT; THES=ASSIGNEE; PLUR=Y	ES; OP=ADJ
	L2	(L1 with evaluat\$)	12
	L1	insulated gate type transistor	263

END OF SEARCH HISTORY

# **Hit List**

First Hit Clear Generate Collection Print Fwd Refs Bkwd Refs Generate OACS

**Search Results -** Record(s) 1 through 12 of 12 returned.

☐ 1. Document ID: US 20040098681 A1

L2: Entry 1 of 12

File: PGPB

May 20, 2004

PGPUB-DOCUMENT-NUMBER: 20040098681

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040098681 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: May 20, 2004

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Yamaguchi, Kenji

Tokyo

JP

US-CL-CURRENT: 716/4

Ì	Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWC	Draw, De
	•												

☐ 2. Document ID: US 20040037148 A1

L2: Entry 2 of 12

File: PGPB

Feb 26, 2004

PGPUB-DOCUMENT-NUMBER: 20040037148

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040037148 A1

TITLE: MIS semiconductor device having improved gate insulating film reliability

PUBLICATION-DATE: February 26, 2004

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Hidaka, Hideto

Hyogo

JP

US-CL-CURRENT: <u>365/223</u>

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KMC Draw. De

☐ 3. Document ID: US 20030113946 A1

Record List Display

L2: Entry 3 of 12

File: PGPB

Jun 19, 2003

PGPUB-DOCUMENT-NUMBER: 20030113946

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030113946 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: June 19, 2003

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Yamaguchi, Kenji

Tokyo .

JΡ

US-CL-CURRENT: <u>438/17</u>

Full	Title	Citation	Front	Review	Classification	Date	Referenc	e Sequences	Attachments	Claims	KWIC	Draw, De
			•	•				•				
***************************************			<del></del> ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,				<u> </u>	•				
	4. I	Documer	nt ID:	US 20	020130679	Al						
L2: E	ntrv	4 of 1	2			E	Tile: I	PGPB		· Sep	19,	2002

PGPUB-DOCUMENT-NUMBER: 20020130679

PGPUB-FILING-TYPE: new

L2: Entry 4 of 12

DOCUMENT-IDENTIFIER: US 20020130679 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Sep 12, 2002

Yamaguchi, Kenji

Tokyo

JΡ

US-CL-CURRENT: 324/769

Full	Titl∈	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWC	Drawt De
 							<u></u>					
	5.	Documei	nt ID:	US 20	020127749	Al						

File: PGPB

PGPUB-DOCUMENT-NUMBER: 20020127749

PGPUB-FILING-TYPE: new

L2: Entry 5 of 12

DOCUMENT-IDENTIFIER: US 20020127749 A1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

PUBLICATION-DATE: September 12, 2002

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Yamaguchi, Kenji

Tokyo

JΡ

US-CL-CURRENT: 438/18; 438/17, 438/275

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KMC Draw De

☐ 6. Document ID: US 20020024059 A1

L2: Entry 6 of 12

File: PGPB

Feb 28, 2002

PGPUB-DOCUMENT-NUMBER: 20020024059

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020024059 A1

TITLE: MIS semiconductor device having improved gate insulating film reliability

PUBLICATION-DATE: February 28, 2002

INVENTOR-INFORMATION:

NAME

CITY

STATE

COUNTRY

Hidaka, Hideto

Hyogo

JΡ

US-CL-CURRENT: 257/<u>189</u>

Full Title Citation Front Review Classification Date Reference Sequences Attachments Chaims KMC Draw De

7. Document ID: US 6816418 B2

L2: Entry 7 of 12

File: USPT

Nov 9, 2004

US-PAT-NO: 6816418

DOCUMENT-IDENTIFIER: US 6816418 B2

TITLE: MIS semiconductor device having improved gate insulating film reliability

DATE-ISSUED: November 9, 2004

INVENTOR-INFORMATION:

NAME

CITY

STATE ZIP CODE

COUNTRY

Hidaka; Hideto

Hyogo

JΡ

US-CL-CURRENT: 365/189.09; 365/185.23, 365/201, 365/226

Full Title Citation Front Review Classification Date Reference Sequences Attectments Claims KMC Draw De

☐ 8. Document ID: US 6727724 B2

L2: Entry 8 of 12

File: USPT

Apr 27, 2004

US-PAT-NO: 6727724

DOCUMENT-IDENTIFIER: US 6727724 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: April 27, 2004

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

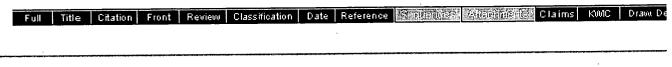
COUNTRY

Yamaguchi; Kenji

Tokyo

JΡ

US-CL-CURRENT: 324/769; 324/719



9. Document ID: US 6649430 B2

L2: Entry 9 of 12

File: USPT

Nov 18, 2003

May 6, 2003

US-PAT-NO: 6649430

DOCUMENT-IDENTIFIER: US 6649430 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Yamaguchi; Kenji

Tokyo

JP

US-CL-CURRENT: 438/17; 438/275

Full   Title	Citation Front Review	Classification	Date	Reference	Saplaines	Alternation.	Claims	KMC	Draw, De
□ 10.	Document ID: US 6	559672 B2						_	

US-PAT-NO: 6559672

L2: Entry 10 of 12

DOCUMENT-IDENTIFIER: US 6559672 B2

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: May 6, 2003

INVENTOR-INFORMATION:

NAME

CITY

STATE ZIP CODE

File: USPT

COUNTRY

Yamaguchi; Kenji

Tokyo

JP

US-CL-CURRENT: 324/769; 324/719



11. Document ID: US 6373274 B1

L2: Entry 11 of 12

File: USPT

Apr 16, 2002

US-PAT-NO: 6373274

DOCUMENT-IDENTIFIER: US 6373274 B1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: April 16, 2002

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

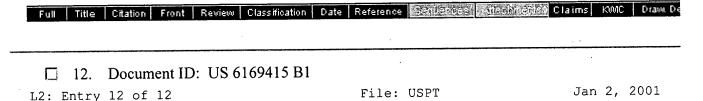
COUNTRY

Yamaguchi; Kenji

Tokyo

JΡ

US-CL-CURRENT: 324/769; 324/719



US-PAT-NO: 6169415

DOCUMENT-IDENTIFIER: US 6169415 B1

TITLE: Characteristic evaluation apparatus for insulated gate type transistors

DATE-ISSUED: January 2, 2001

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Yamaguchi; Kenji

Tokyo

JΡ

US-CL-CURRENT: 324/769; 324/719

Title Citation Front Review Classification Da	ate Reference Schlenisch Chaims KWI
Generate Collection Print	Fwd Refs Bkwd Refs Generate (
Generale Confection	wu neis Ditta field 2 Conouce
	Deguments
Term	Documents
EVALUAT\$	Documents
	0 26